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Patterning issues for the fabrication of sub-micron memory capacitors' electrodes

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Abstract

This paper describes some of the key issues associated with the patterning of metal electrodes of sub-micron (especially at the critical dimension (CD) of 0.15 μm) dynamic random access memory devices. Due to reactive ion etching lag, the Pt etch rate decreased drastically below the CD of 0.20 μm and thus K-th storage node electrode with the CD of 0.15 μm could not be fabricated using the Pt electrodes. Accordingly, we have proposed novel techniques to surmountly-the above difficulties. The Ru electrode cannot for the stack-type structure is introduced and alternative multischemes based on the introduction of the concave-type selfstructure upto using semi-Pt or Ru as an electrode material are outlined respectively.

Keywords: Platinum; Ruthenium; Etching; Critical dimension; Reactive ion etching lag

1. Introduction

The usage of barium strontium titanate (BST) capacitor and the lead zirconium titanate (PZT) capacitor have recently been considered, respectively, in the fabrication of ferroelectric random access memory device and dynamic random access memory (DRAM) device. As an electrode material for both BST and PZT capacitors, various materials such as platinum (Pt), iridium (Ir), ruthenium (Ru), and ruthenium oxide (RuO_2) have been studied.

In order to use the Pt as an electrode material in the stacked capacitor cell structure successfully (Fig. 1), Pt etching technique in order to pattern the bottom electrode needs to be developed. However, as Pt has a low reactivity and its etching products have low vapor pressures [1,2], the etching of Pt proceeds by physical sputtering, resulting in low etch selectivity of Pt to mask and unwanted sidewall redeposition [3–5]. As a result, Pt has a low etch slope and thus the adjacent nodes are connected with Pt, the bottom Pt storage nodes cannot be separated from their adjacent storage nodes.

In this paper, we report the Pt electrode etching for 0.15 μm-CD storage node pattern, revealing that the above method is not suitable to the stacked storage node pattern at the CD of 0.15 μm and below. Accordingly, we propose to use the Ru electrode in the stack-type storage node structure and to introduce a concave-type storage node structure.

2. Etching issues of Pt electrode for stack-type capacitor

In order to systematically investigate the effect of the space CD on the etch rate and etch slope of Pt, the line and space pattern with the space CD ranging from 100 to 350 nm, was used (not shown here). The etch rate decreases drastically below the CD of 200 nm, resulting in almost zero etch rate at the space CD of 150 nm. The Pt etch slope also decreases with decreasing CD in the pattern.

From the above observations, we surmise that the limitation of Pt etching at small CD is related to reactive ion etching (RIE) lag phenomena. We suppose that the real etching (physical sputtering) and the redeposition occur simultaneously during the etching process. When the space CD is small and thus the aspect ratio is big enough, the sputtered Pt atoms mostly redeposit to sidewalls rather than flying out of the pattern.

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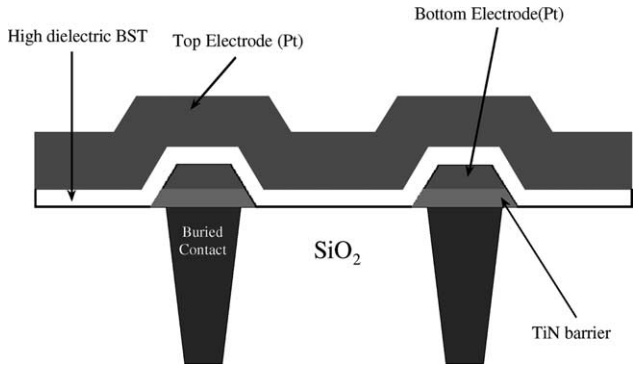


Fig. 1. Schematics of a stack-type Pt/BST/Pt capacitor strcuture.

A storage node pattern was used in our experiments. The sample structure was bottom SiO_2/titanium nitride (TiN) 500 Å/Pt 2000 Å/mask Ti 600 Å/mask SiO_2 3000 Å/photoresist (PR). After patterning SiO_2, which is a first mask for Pt etch, the PR was removed. The Ti layer, which is a second mask for underlying Pt, was patterned by the Ar/Cl_2 chemistry using the SiO_2 mask. Schematic of a RIE for Pt etching is shown in our previous work [6]. In the Pt etching process, the O_2 gas was used as a main etchant. The Pt etch process consists of a main etch step stopped at end point detection and an over etch step to remove the Pt residues. Then the barrier TiN layer was removed by etching with Ar and Cl_2 gases.

Fig. 2a shows the tilted cross-section of the storage node bottom electrode along the short-axis, at the CD of 0.29 μm. Fig. 2b and c shows the cross-sections of the storage node bottom electrode along the short-axis, at the CD of 0.15 μm. In case of the CD of 0.15 μm, the TiN bottom barrier is not exposed and the space CD is maintained to be zero even by over etch, indicating that the Pt layer is connected along the short-axis (Fig. 2b). In this case, after removing TiN barrier layer, the bottom space between two adjacent nodes is not wide enough and the following steps of the BST deposition and the top electrode Pt deposition cannot be accomplished. Furthermore, by excessive overetch, the mask Ti layer is completely eroded and the volume of the Pt node itself becomes significantly reduced (Fig. 2c). Therefore, the top area of the storage node is relatively small and it cannot guarantee a sufficient capacitance area and cannot obtain a required storage capacity per cell.

3. Etching issues of Ru electrode for stack-type capacitor

Ru is expected to be patterned by chemical etching because the volatile etch product can be produced [7,8]. Fig. 3 shows the cross-sectional SEM images of the Ru electrode pattern etched in helicon plasma. The sample structure was substrate/TiO_2 600 Å/Ru 4000 Å/SiO_2 mask with a CD of 0.15 nm. Since oxygen gas was the main etchant, SiO_2 mask, instead of PR mask, was used for patterning Ru. Fig. 3a and b show the images etched using O_2 gas and O_2/Cl_2 (10% Cl_2) gas, respectively, for 1 min. The Ru etch rates using O_2 gas and O_2/Cl_2 gas are 50 Å/min and 450 Å/min, respectively, revealing that the addition of Cl_2 gas is crucial in efficient Ru etching. We have applied the high density plasma, such as helicon plasma [9] and inductively coupled plasma [10], to etch the Ru electrode and have obtained the maximum Ru etching slope of about 86°. The optimized Ru etching

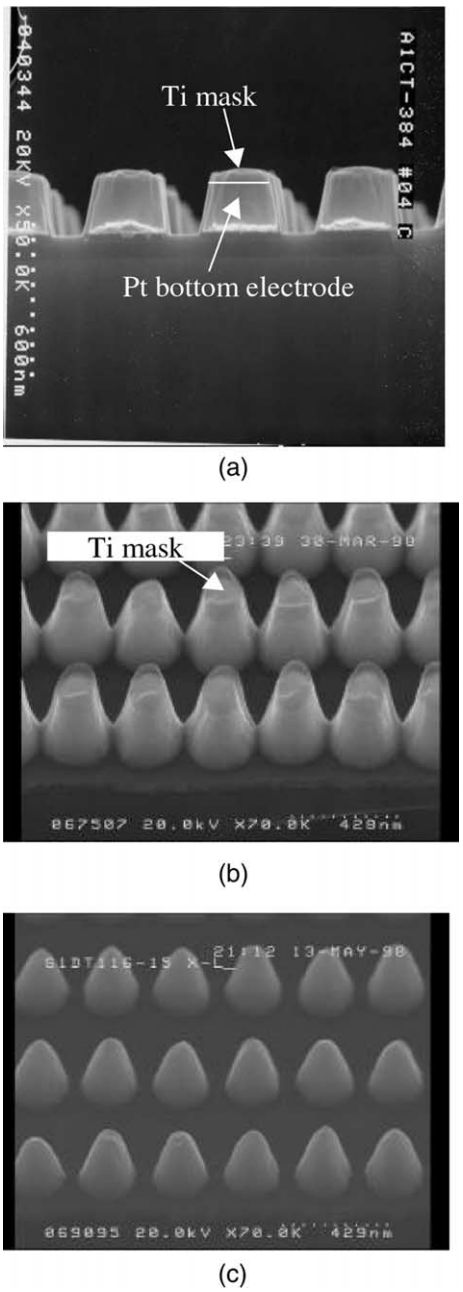


Fig. 2. SEM images of the Pt etching profile at the storage node patterns (a) with a CD of 0.29 μm, (b) with a CD of 0.15 μm. By overetch, the Pt electrodes are connected (c) with a CD of 0.15 μm. By excessive overetch, the Ti mask is completely eroded, resulting in the reduced Pt electrodes.

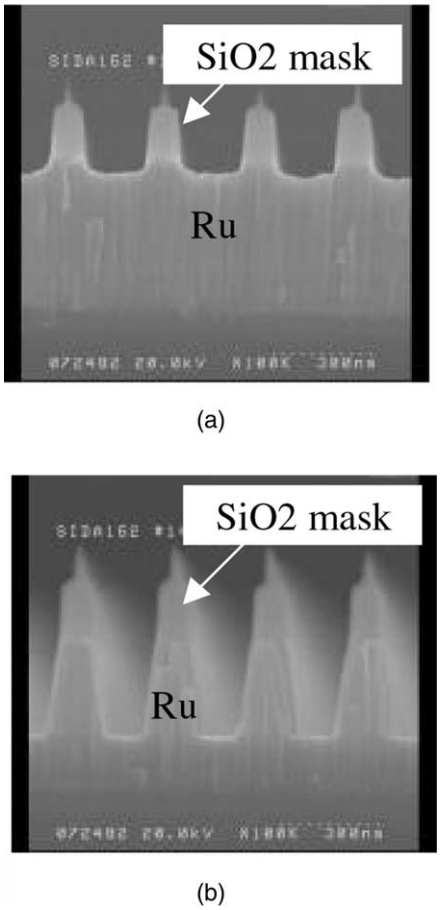


Fig. 3. SEM images of Ru etching profiles at a storage node pattern with a CD of 0.15 μm, (a) using a O_2 gas and (b) using O_2/Cl_2 gases.

rates and Ru to SiO_2 etch selectivity using the helicon etcher are measured to be about 550 Å/min and 5.5, respectively.

When the etching process has a sufficient etch selectivity of Ru to SiO_2, SiO_2 mask residues are remaining on top of the Ru electrode, even after completing the etching process. We surmise that the mask SiO_2 layer reacts with the Ru surface by the supplied thermal energy during etching process and thus the adhesive RuO_x-type compounds are generated between the mask SiO_2 and Ru surface. In order to remove the SiO_2 mask residues, we have applied the wet etching technique using a aqueous hydrofluoric acid (HF) solution, revealing that the removal process of the mask residues cannot be controlled. Accordingly, we have applied the plasma etching using Ar/CHF_3 system, revealing that the mask residues of the irregular shapes are remained even by 100% overetch. By applying the high-RF power etching process, the SiO_2 mask sidewall residues on top of Ru electrode could be removed but the Ru etching slope is lowered during the mask removal etching, probably due to the resputtering of Ru atoms. Further study is necessary to obtain the high enough Ru etching slope with no SiO_2 mask residues.

4. Etching issues of Pt electrode for concave-type capacitor

To avoid the difficulties of high aspect ratio Pt etching, we suggest to introduce a concave-type storage node pattern. The fabrication procedure of the concave capacitor cell is shown in Fig. 4. After forming the concave-type structure by etching SiO_2 layer, we deposit the bottom electrode Pt layer and subsequently coat the protective PR layer on top of the Pt bottom electrode. Since only the Pt layer inside the hole of the concave structure is utilized as the bottom electrode, the PR layer and subsequently the bottom electrode Pt layer outside the hole is removed.

For the PR etchback process, the dual frequency RIE with the combination of the 13.56 MHz power and the 450 kHz power is used in order to obtain a high energy ion bombardment. The chamber pressure was 30 mTorr with the O_2 gas as a main etchant. Fig. 5a and b show the profiles of the concave-type structure before and after the etchback of PR layer, respectively. We reveal that

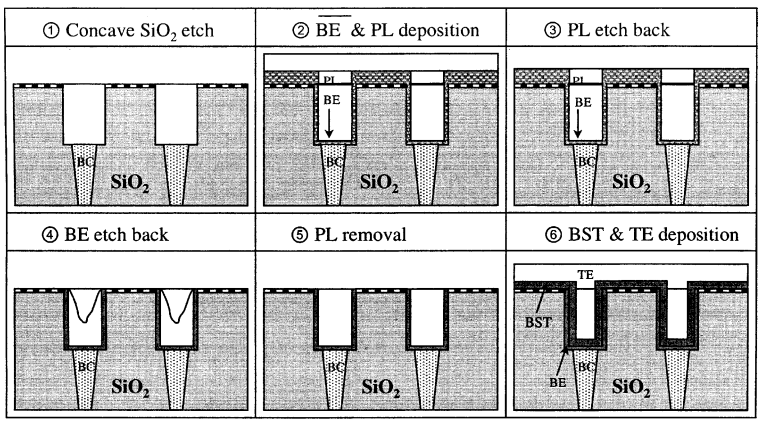
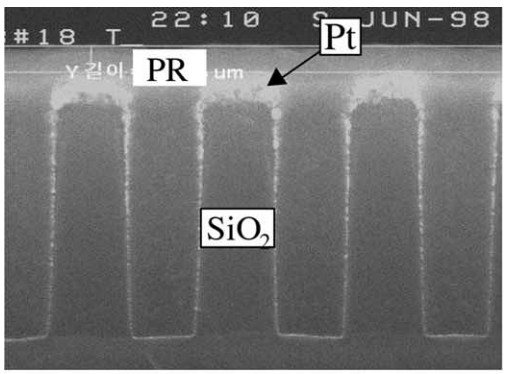
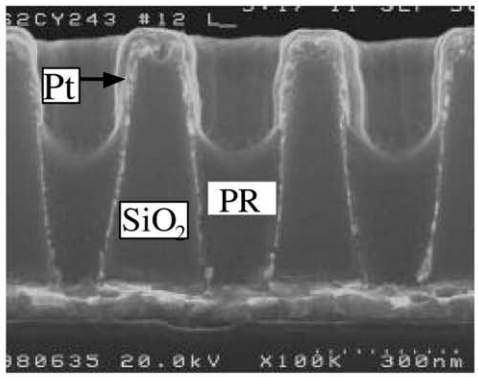


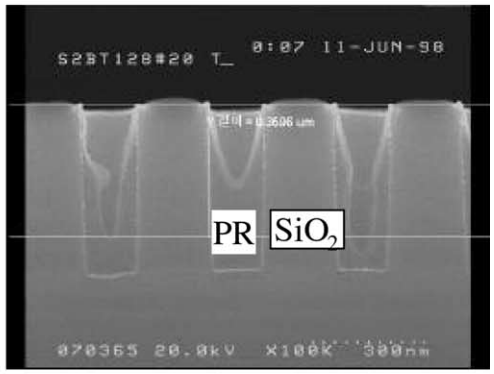
Fig. 4. The fabrication sequence of concave-type capacitor ('BC', 'TE', 'BE' and 'PL' represent the buried contact, the top electrode layer, the bottom electrode layer, and the protecting layer, respectively).



(a)



(b)



(c)

Fig. 5. Concave-type structure with Pt electrodes (a) before and (b) after the etchback of photoresist (PR) layer. (c) After the etchback of Pt layer.

the Pt layer outside the concave hole is slightly exposed after the etchback process and the Pt layer is not eroded due to the sufficiently high (~30 mTorr) etching pressure and resulting low Pt etch rate. The height of the remaining PR inside the concave hole should be optimized. If the height is too high, some concave holes will have an unwanted PR layer on top of the Pt layer outside the hole. If the height is too low, the PR layer protecting the bottom Pt electrode may be completely eroded during the following Pt etchback process and the bottom Pt layer will be damaged.

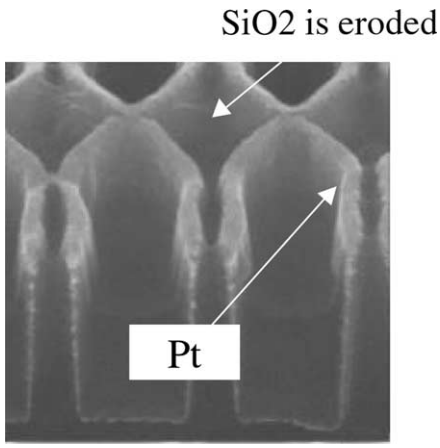
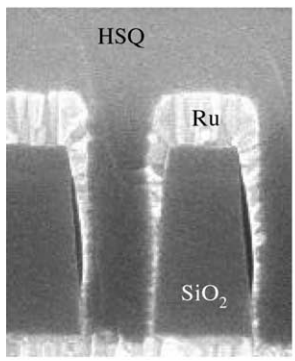
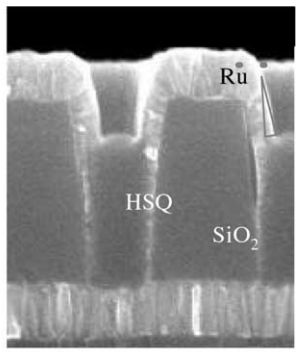


Fig. 6. Concave-type Pt electrode profiles when the SiO_2 is excessively eroded.

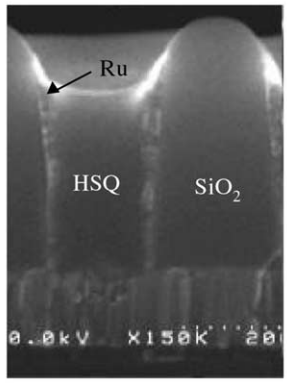
In order to separate the Pt layer inside each concave hole and to form a bottom electrode, we remove the Pt layer deposited outside the concave hole by an etchback process (Fig. 5c). We etched the Pt, PR, and SiO_2 layer concurrently and etch rates of the three materials are recommended to be almost equal. The dual frequency RIE is used with the flow of Ar/Cl_2 gas. In this step, if the Pt to SiO_2 etch selectivity are not sufficiently high,



(a)



(b)



(c)

Fig. 7. SEM images of Ru concave-type structure (a) before and (b) after the etchback of hydrogen silsesquioxane (HSQ) layer. (c) After the etchback of Ru bottom electrode layer.

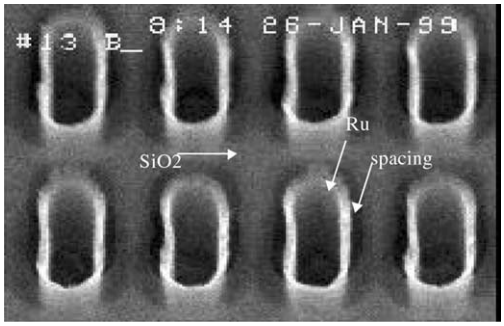


Fig. 8. SEM image of the Ru concave-type structure after removing the HSQ with the HF solution.

otherwise the SiO_2 between the nodes are excessively etched (Fig. 6). After completing the Pt etchback process, we remove the remaining PR inside the concave hole, and subsequently deposit the BST layer and the top electrode Pt layer.

5. Etching issues of Ru electrode for concave-type capacitor

After forming a concave structure with SiO_2, the bottom electrode Ru layer is deposited and subsequently the protective hydrogen silsesquioxane (HSQ) layer is coated (Fig. 7a). In order to reduce the thickness of HSQ layer and expose the top part of the Ru layer, the HSQ etchback is performed (Fig. 7b).

In order to separate the Ru layer inside each concave hole and to form a bottom electrode, we remove the Ru layer deposited outside the concave hole by etchback process. The dual frequency RIE is used in order to obtain a high energy ion bombardment. The chamber pressure is 30 mTorr and the O_2 and Cl_2 gas with the $(Cl_2/O_2 + Cl_2)$ gas flow ratio of 0.2 is used. In the Ru etchback process, the Ru to HSQ etch selectivity needs to be sufficiently high, otherwise the HSQ layer inside the hole will be eroded away. Fig. 7c shows the profiles of the concave-type structure after the etchback of Ru bottom electrode layer.

Fig. 8 shows the profiles of the concave-type structure after the removal of the remaining HSQ layer using the aqueous HF solution, which has an enough HSQ to SiO_2 etch selectivity. The SEM image indicates that the very small spacing can be generated between the Ru and the surrounding SiO_2 during the following HF treatment, probably due to the penetration of HF solution. In order to prevent the penetration of the HF solution, we are developing various techniques, including the insertion of the blocking thin layer on top of the SiO_2 layer. We subsequently deposit the BST layer and the top electrode Ru layer, resulting in the complete fabrication of the capacitor structure.

6. Summary

This paper describes some of the key issues associated with the patterning of metal electrodes of sub-micron (especially at 0.15 μm) DRAM devices, by employing the novel techniques. The Ru electrode for the stack-type structure is fabricated with an acceptable etching slope but the removal of the remaining SiO_2 mask is a challenging problem. Alternative schemes based on the introduction of the concave-type structure using Pt or Ru as an electrode material are introduced and issues in patterning the Pt or Ru bottom electrodes are discussed.

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