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Temperature Effect on Tungsten Etching Using a Cl_2/O_2 Helicon Discharge

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The effect of temperature on tungsten (W) etching has been investigated using the Cl_2/O_2 plasmas in a helicon etcher. The etch rates of W and the wafer temperature were increased by increasing the source power and the bias power and by decreasing the pressure, indicating that the W etching is controlled by the temperature. The use of Cl_2/O_2 plasmas to successfully pattern W-metal gate electrodes has been demonstrated.

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I. INTRODUCTION

As device dimensions become smaller, the gate resistance becomes higher, so the usage of metal gate electrodes with low resistivity should be considered. Accordingly, metal gate electrodes, such as W, titanium nitride (TiN), and ruthenium oxide (RuO_2), have been reported to be promising candidates [1–6]. Among the metallic gate materials, W has been considered appropriate due to its high thermal stability, good corrosion resistance, and high process compatibility.

Although metal gate electrodes using W have been investigated [1–3], there are rare reports on the etching of W. In addition, several researchers have investigated the helicon discharge and its application to the etching of various materials such as silicon (Si) and silicon dioxide (SiO_2) [7–11]. In this paper, we employ a helicon plasma to investigate the characteristics of W etching using a Cl_2/O_2 system. We suggest to increase the W etch rate by elevating the wafer temperature.

II. EXPERIMENT

A schematic diagram of the m=0 helicon plasma reactor used in this study is described in Fig. 1. Helicon wave plasma sources were operated at an excitation frequency of 13.56 MHz. The diameter of the process chamber, which was covered by 24 cusp magnets along the chamber axis, was 350 mm. The helium pressure was 20 Torr, and both the inner and the outer coil currents were 40 Amperes. During etching, the source power was 500 ∼ 2000 Watts (W), the bias power was 0-400 W, the magnetic field was 100 ∼ 200 Gauss, and the total gas flow rate of Cl_2/O_2 system was set to 50 standard cubic centimeters per minute (sccm).

Blanket wafers were used to measure the etch rates of W, polycrystalline (poly) Si, and SiO_2 because the W/ poly-Si and the poly-Si/ oxide etch selectivity can not be measured accurately for patterned wafers. Patterned wafers with a critical dimension (CD) of 0.17 nm were used to demonstrate the formation of a metal gate electrode. A poly-Si layer is inserted between W/WN_x and gate oxide because W/WN_x has poor adhesion with the underlying gate oxide. WN_x is inserted between W and poly-Si to prevent the generation of an unwanted WSi_x layer. The metal gate electrode had the following structure: a 2000-Å SiO_2 mask/ 1000-Å W / 100-Å WN_x

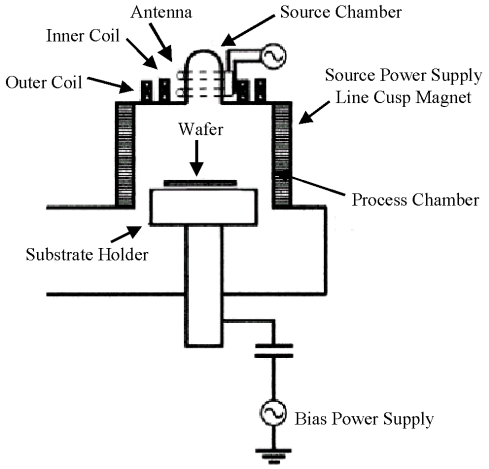

Fig. 1. Schematic diagram of an m=0 helicon plasma reactor.

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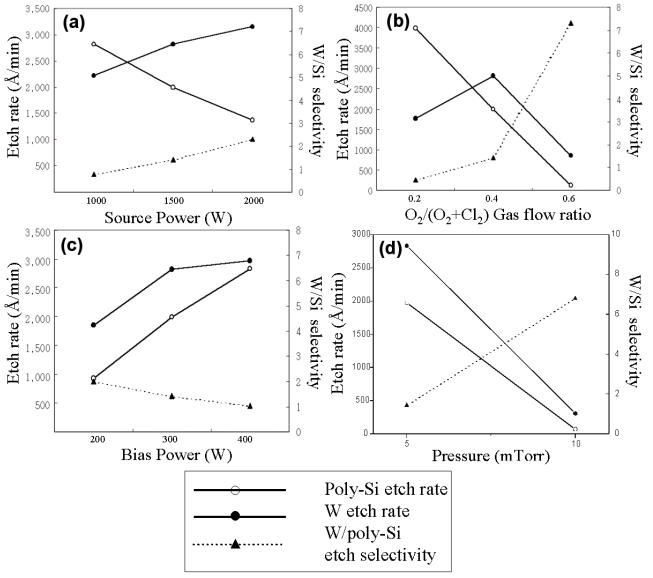

Fig. 2. Variations of the W etch rate, the poly-Si etch rate, and the etch selectivity of W over poly-Si with the (a) source power, the (b) $O_2/(O_2 + Cl_2)$ gas flow ratio, the (c) bias power, and the (d) pressure.

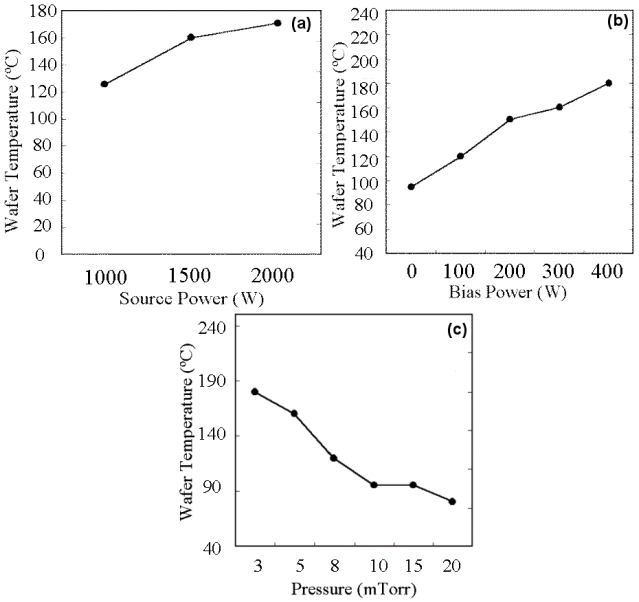

Fig. 3. Variations of the wafer temperature with the (a) source power, the (b) bias power, and the (c) pressure.

/ 1000-Å poly-Si / 60-Å gate oxide / Si substrate.

The cathode temperature before etching was set to 20 °C by using a chiller. An irreversible thermal tape was used for measuring the wafer temperature in-situ during etching processes. Because the wafer temperature depends on the etching time, the etch time was fixed to 30 seconds in this study. A scanning electron microscope (SEM) (Hitachi S-4700) was used to characterize the fabricated metal gate electrode.

III. RESULTS AND DISCUSSION

In order to investigate the feasibility of forming a W/WN_x/poly-Si structure with a vertical profile, we investigated the etch rates of W and poly-Si by varying the process conditions. Figure 2 shows the variations of the W etch rate, the poly-Si etch rate, and the etch selectivity of W over poly-Si with the process parameters. At the standard etching condition, the source power was 1500 W, the bias power was 300 W, and the pressure was 5 mTorr, with a gas-flow ratio of $Cl_2/O_2 = 30 : 20$ (sccm) for 60 seconds. The source power and the bias power ranged from 1000 to 2000 W and from 200 to 400 W, respectively. The pressure was $5 \sim 10$ mTorrs and the $O_2/(Cl_2 + O_2)$ gas flow ratio ranges from 0.2 to 0.6 with a total flow rate of 50 sccm. With increasing source power, the poly-Si etch rate decreased and the W etch rate increased, resulting in an increase of the W to poly-Si etch selectivity. With increasing bias power, both the poly-Si and the W etch rates increased, resulting in a slight decrease of the W to poly-Si etch selectivity. The W etch rate was maximized at O_2 and Cl_2 flow rates of 20 and 30 sccm, respectively, implying the possible formation of volatile WOxCly compounds as an etch product. In spite of that, with increasing O_2 / $(Cl_2 + O_2)$ gas flow ratio, the etch selectivity of W over poly-Si increased due to a significant decrease in the poly-Si etch rate. The W etch rate was very low at high (10 mTorr) pressure and increased with decreasing pressure. We surmise that decreasing the pressure increased the wafer temperature by reducing the collision rates in the sheath region, thereby increasing the ion bombardment energy. In our experiments, the effect of increased temperature dominated the effect of reduced radical density at lower pressure, resulting in an increased W etch rate.

We used blanket W wafers to measure the wafer temperature under vatious process conditions (Fig. 3). As the pressure was decreased from 20 mTorr to 3 mTorr, the wafer temperature increased from 85 °C to 180 °C. As the source power was increased from 1000 to 2000 W, the wafer temperature increased from 125 °C to 170 °C. As the bias power was increased from 0 W to 400 W, the wafer temperature increased from 95 °C to 180 °C. The above observations reveal that the wafer temperature increases with increasing source power, increasing bias power, and decreasing pressure. By comparing Fig. 3 with Fig. 2, regarding the experimental results for various source powers, bias powers, and pressures, we find that the W etch rate increases with increasing wafer temperature.

Figure 2(d) shows that an optimum Cl_2 / $(Cl_2 + O_2)$ gas flow ratio exists for a maximal W etch rate, probably due to the formation of volatile WO_xCl_y compounds from the reaction of W with the Cl and the O

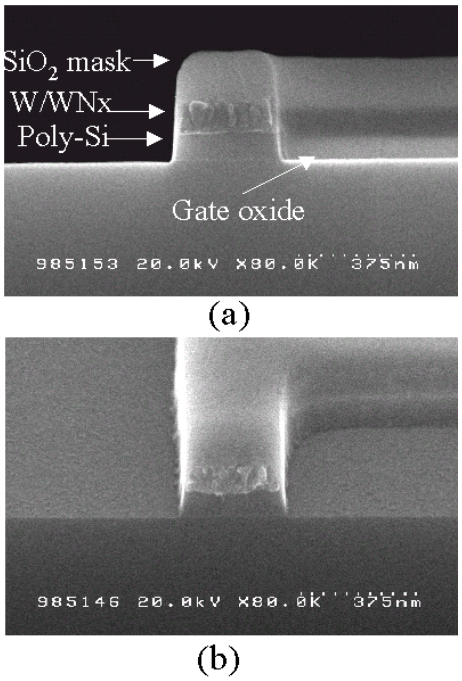

Fig. 4. (a) Cross-sectional view and (b) tilted view of the W gate electrode pattern etched with an O_2/Cl_2 plasma.

species in the plasma. We surmise that the formation of WO_xCl_y compounds is crucial because the boiling point of $WOCl_4$ is about 227 °C, which is much lower than the boiling points or sublimation temperatures of WCl_x and WO_x compounds: The boiling points of tungsten chlorides such as WCl_5 and WCl_6 are about 276 °C and 347 °C, respectively, and tungsten oxides such as WO_2 and W_2O_5 sublimate at temperatures higher than 800 °C. The enhancement of the W etch rate with increasing temperature is possibly due to an enhancement of compound-forming reactions at higher temperatures. Also, since the W etch rate increases with increasing bias power, physical sputtering by energetic ions may play a role in efficient W etching. We surmise that the sputtering ions help to increase the wafer's surface temperature by colliding with the substrate and, thus, activating the chemical reactions. In addition, the ion bombardment itself causes the volatile etch products to be more easily desorbed from the surface. More systematic study is necessary to reveal the detailed mechanism of W etching. As mentioned earlier, the standard etching conditions were a source power of 1500 W, a bias power of 300 W, and a pressure of 5 mTorr, with a gas flow ratio of $Cl_2/O_2 = 30 : 20$ (sccm) for 60 seconds, resulting in an etch selectivity of W to poly-Si of about 1.4 and an etch selectivity of poly-Si to SiO_2 of about 9.7. The wafer surface temperature during etching was measured to be 160 °C. Figure 4 shows the etch profiles of the gate electrode pattern. A straight and almost vertical etch profile without sidewall residues and defects was uniformly produced. We observe no post-etch pitting of or defects in the gate oxide throughout the wafer.

IV. CONCLUSIONS

We studied the dependence of W etching on various parameters. The W etch rate is increased by increasing the source power, by increasing the bias power, and by decreasing the pressure. Since the W etch rate increases with increasing wafer surface temperature, the wafer temperature is a crucial factor for efficient W etching. The dependence of the W etch rate on the O_2 / (Cl_2 + O_2) gas-flow ratio, as well as on wafer temperature, indicates that chemical reactions play a crucial role in W etching. Patterning of a W/WN_x/poly-Si structure using a Cl_2/O_2 helicon plasmas was demonstrated, and the structure showed an almost vertical profile and no pitting of the gate oxide.

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