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Investigation into the patterning of a concave-type Pt electrode capacitor using the reactive ion etching method

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Abstract

We have developed a concave-type Pt electrode capacitor to overcome the limitations of the conventional stack-type capacitor in a small critical dimension pattern. We deposited a Pt layer on the concave-type structure made by the patterning of SiO_2 and subsequently separated the adjacent nodes by the etch-back process with a photoresist as a protecting layer. We summarize the issues regarding patterning in the reactive ion etching system for fabrication of a concave-type capacitor.

Keywords: Platinum; Etching; Concave; Critical dimension

1. Introduction

To increase the storage capacity per cell for 4 Giga-bit dynamic random access memory (DRAM) and beyond, the use of a barium strontium titanate (BST) capacitor has been considered. Various materials, such as platinum (Pt), iridium (Ir), ruthenium (Ru), and ruthenium oxide (RuO_2), have been examined as electrode material for the BST capacitor. Among these, Pt is most appropriate because of its good oxidation resistance, high electrical conductivity, and low leakage current characteristics [1,2].

In order to use Pt as an electrode material in the stacked capacitor cell structure, a Pt etching technique, in order to pattern the bottom electrode, has been developed [3–5]. However, as Pt has low reactivity and its etching products have low vapor pressures [6,7], the etching of Pt proceeds by physical sputtering. Accordingly, Pt has a low etch slope and, thus, as the adjacent nodes are

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connected to Pt, the bottom Pt storage nodes cannot be separated from their adjacent storage nodes, especially in a very low critical dimension (CD) pattern [8–11].

In order to allow for lateral shrinkage of the cell size while maintaining the required cell capacitance without employing difficult Pt electrode etching, we have developed a concave-type cell structure [12], and show that the above method is suitable for a storage node pattern in the CD of 0.17 μm and below.

2. Experimental

The fabrication sequence of the concave-type Pt/BST/Pt capacitor is shown in Fig. 1. After forming a concave structure with SiO_2, the bottom electrode Pt layer is deposited. The protective photoresist (PR) layer is deposited, and then etch-back is performed to isolate the Pt layer of each concave structure. After removing the remaining PR by ashing, BST and the top electrode Pt layer are deposited to form a capacitor.

A schematic of the reactive ion etcher (RIE) used in this work is shown in our previous work [12]. The combination of high-radio-frequency power (HRF), 13.56 MHz, and low-radio-frequency power (LRF), 450 kHz, in addition to the low operating pressure (< 10 mTorr), results in high-energy ion bombardment. The SiO_2 etching was performed to make a concave structure and a mixture of Ar, CF_4, and CHF_3 gas was used as etchant. In the Pt etch-back process, Ar gas and Cl_2 gas were employed as etchant. In the photoresist etch-back process, O_2 gas was used as etchant.

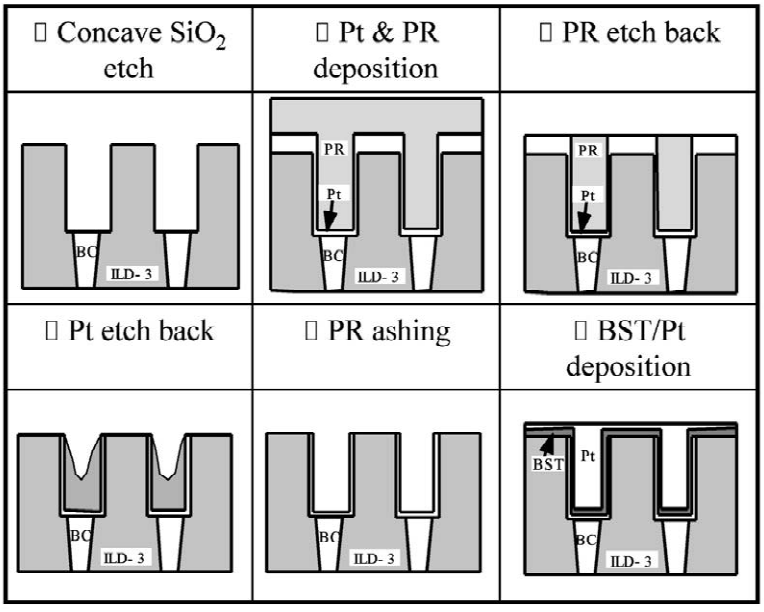

Fig. 1. Fabrication sequence for the concave-type Pt/BST/Pt capacitor (ILD-3 represents the inter-layer dielectrics of SiO_2 and ''BC'' represents the buried contact).

3. Results and discussion

3.1. SiO_2 etching to form a concave-type structure

Fig. 2 shows the etching profile of the concave structure in a pattern with a CD of 0.17 μm using an $Ar/CF_4/CHF_3$ plasma. The SiO_2 to PR etch selectivity increases on increasing the CHF_3 gas flow rate, regardless of the HRF power and pressure. The SiO_2 to PR etch selectivity increases on increasing the HRF power, regardless of the CHF_3 gas flow rate and pressure. Since a high SiO_2 to

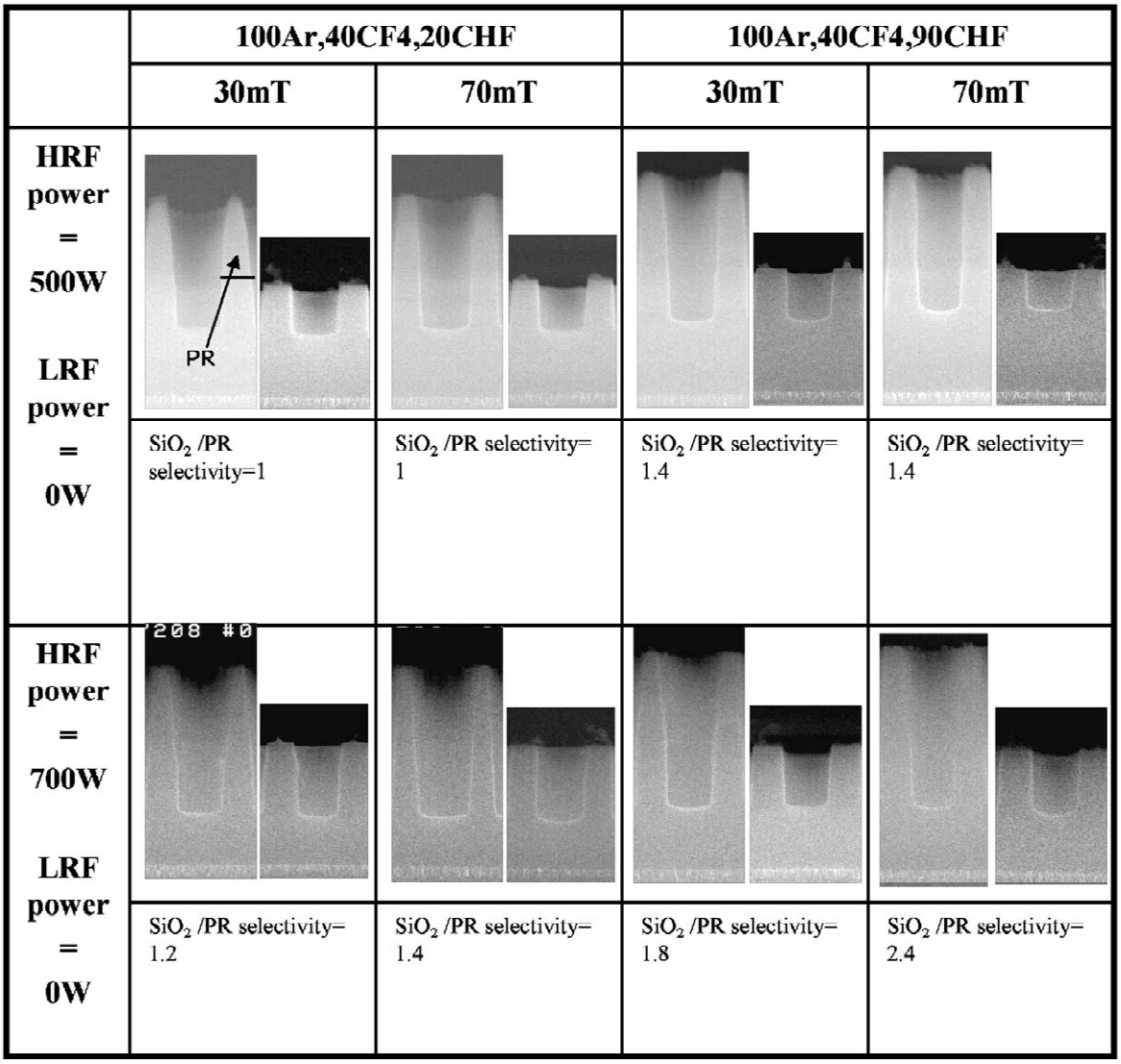

Fig. 2. Etching profile of the SiO_2 concave structure in a pattern with a CD of 0.17 μm using an $Ar/CF_4/CHF_3$ plasma. The left- and right-hand sides of each figure represent the etching profile before and after ashing, respectively.

PR etch selectivity is crucial for obtaining a vertical profile with a high aspect ratio, we used etching conditions with a HRF power of 700 W, a LRF power of 0 W, a CHF_3 flow rate of 90 sccm, and a pressure of 70 mTorr, resulting in a SiO_2 to PR etch selectivity of 2.4. In order to evaluate the effect of the LRF power, we changed it from 0 to 200 W, with an HRF power of 700 W and a pressure of 70 mTorr. The SiO_2 to PR etch selectivity decreases on increasing the LRF power from 0 to 200 W.

We performed experiments forming the concave structure in a CD of 0.15 μm. Fig. 3 shows an image of the top view of the concave structure etched using the $Ar/CF_4/CHF_3$ plasma with etch depth varying from 2600 to 5600 Å. Fig. 3 reveals that striation starts to occur as the etch depth becomes greater than 4000 Å, probably due to erosion of the PR mask between adjacent nodes along the short axis. A more systematic study is necessary to increase the SiO_2 to PR etch selectivity in a pattern with a CD of 0.15 μm.

3.2. Photoresist etch-back process

After forming the concave-type structure by etching the SiO_2 layer, we deposited a Pt layer, which is used as the bottom electrode of the capacitor. On top of this, we coated the PR layer to protect the underlying Pt layer. Since only the Pt layer inside the hole of the concave structure is utilized as the bottom electrode, the coated PR layer and subsequently the Pt layer outside the hole needs to be removed. For our etch-back process, the chamber pressure was 30 mTorr and the O_2 gas flow rate was 50 sccm, with a HRF (13.56 MHz) power and LRF (450 kHz) power of 600 and 0 W, respectively.

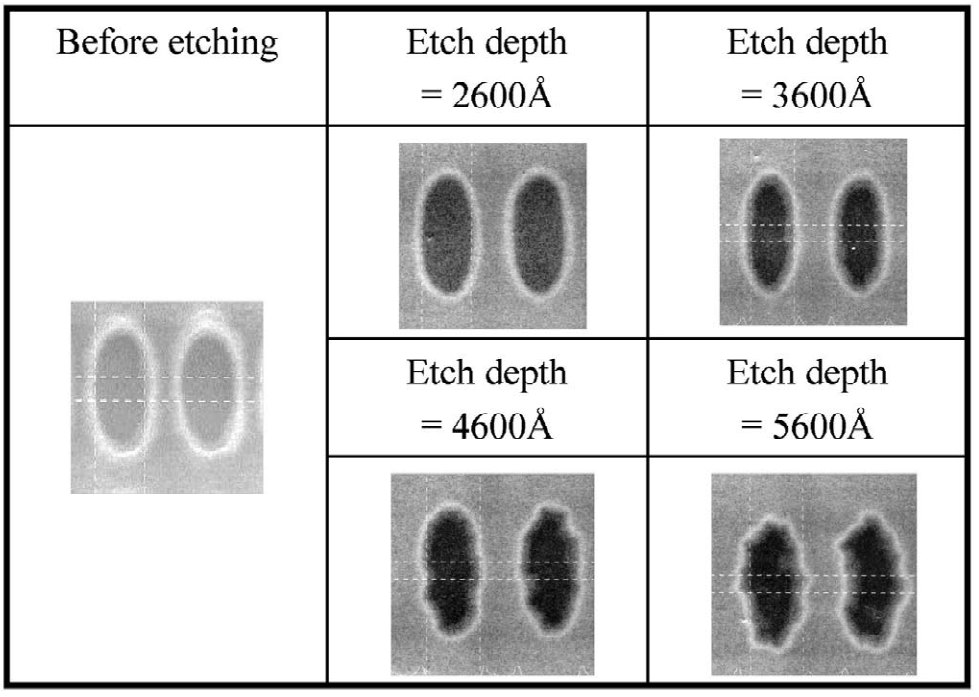

Fig. 3. Top view of the profile of the SiO_2 concave structure with varying etching depth.

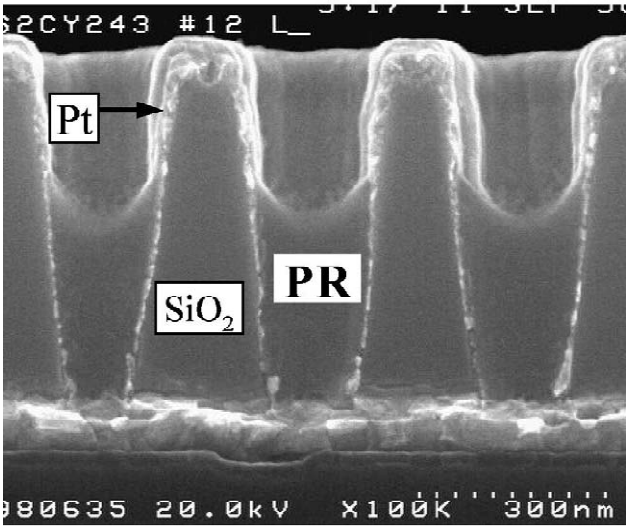

Fig. 4. Concave-type structure (a) before and (b) after etch-back of the photoresist (PR) layer.

The resulting PR etch rate and etch uniformity are about 6200 Å/min and less than 5%, respectively. Fig. 4 shows the profiles of the concave-type structure after etch-back of the PR layer. We can see that the Pt layer outside the concave hole is slightly exposed after the etch-back process and that the Pt layer is not eroded due to the sufficiently high ($\sim$30 mTorr) etching pressure and resulting low Pt etch rate.

The height of the remaining PR inside the concave hole should be optimized. If the height is too high, some concave holes will have an unwanted PR layer on top of the Pt layer outside the hole. If the height is too low, the PR layer protecting the bottom Pt electrode may be completely eroded during the following Pt etch-back process and the bottom Pt layer will be damaged.

3.3. Pt etch-back process and separation of Pt electrodes

In order to separate the Pt layer inside each concave hole and to form a bottom electrode, we removed the Pt layer deposited outside the concave hole using the etch-back process. We etched the Pt, PR, and SiO_2 layers concurrently and etched up to the point where the height of the etched SiO_2 layer was about 80% of the original height.

In our experiment, we observed air pockets inside the PR in the concave hole. The presence of air pockets will promote the erosion of PR and, thus, the bottom Pt layer inside the hole will be exposed. Fig. 5 shows that a Pt polymer is generated on the bottom of the hole by unwanted etching of Pt. Since this generated Pt polymer cannot be removed during the following ashing and strip process and, thus, the bottom Pt electrode is disabled, we suggest that the PR layer should be deposited without generating air pockets inside. Since generation of air pockets is related to the high speed of revolution of the PR coater, we are developing a technique to use a low-viscosity photoresist without sacrificing deposition uniformity.

In this step, the Pt to PR etch selectivity needs to be sufficiently high, otherwise the PR layer inside the hole will be eroded away. Fig. 6 shows the change of the profiles depending on the etch-back

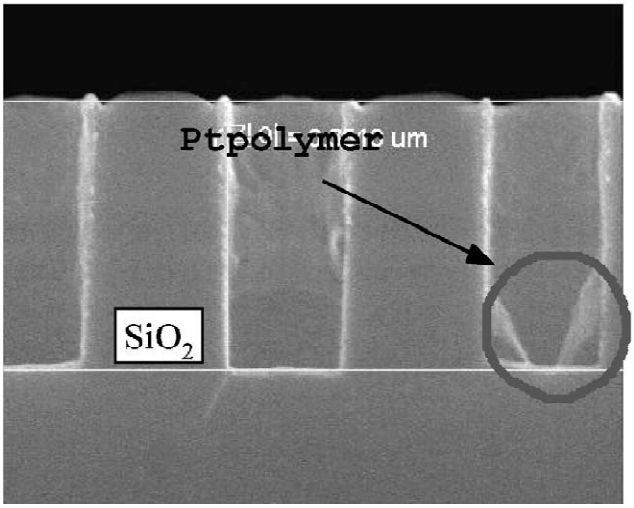

Fig. 5. Pt polymer is generated on the bottom of the hole by excessive etching of Pt.

conditions with varying process variables. The etching pressure is set to 5 mTorr because the Pt is mainly etched by physical sputtering and, thus, the high pressure reduces the Pt etch rate. When the LRF power is 0 W and the Ar and Cl_2 gas flow rates are 20 and 5 sccm, respectively, the Pt to PR etch selectivity is 1.9 (Fig. 6a). However, if the Pt to PR etch selectivity is relatively low (Fig. 6b), excessive erosion of PR inside the concave hole is observed.

After the Pt layer outside the concave hole was removed and, thus, the bottom electrodes were separated, we added an over-etch step considering the etch uniformity. Fig. 7a shows the profile after the etch process only. Fig. 7b shows the profile using an over-etch step with the same conditions as the main etch step, revealing that the SiO_2 between the nodes is excessively etched. Therefore, we used an over-etch step with a HRF and LRF power of 600 and 100 W, respectively, with a pressure of 30 mTorr, and with Ar and Cl_2 flow rates of 20 and 10 sccm, respectively. In this over-etch process, the etch rates of Pt, SiO_2, and PR are about 1000 Å/min, irrespective of the etching material. Fig. 7c reveals that the SiO_2 between the nodes is not eroded excessively, and the surface of the SiO_2 is relatively smooth. After completing the Pt etch-back process, we removed the remaining PR inside the concave hole, and subsequently deposited the BST layer and the top electrode Pt layer, forming the capacitor structure.

4. Conclusions

To avoid the difficulties of high aspect ratio Pt etching, we suggest the introduction of a concave-type storage node pattern. In order to form a concave structure with SiO_2, we tried to increase the SiO_2 to PR etch selectivity. We deposited a protective PR layer and then etch-back was performed to isolate the Pt layer of each concave structure. The height of the remaining PR inside the

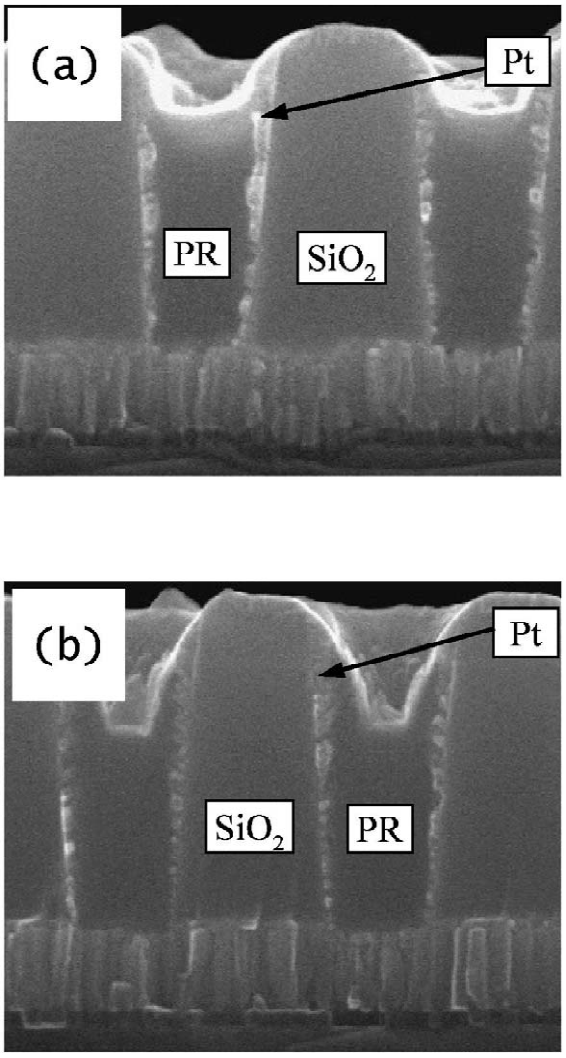

Fig. 6. Change of the profiles depending on the etch-back conditions. (a) The Pt to PR etch selectivity is about 1.9. (b) The Pt to PR etch selectivity is low.

concave hole was optimized. The relative etch rates of Pt, PR, and SiO_2 were optimized in the Pt etch-back process.

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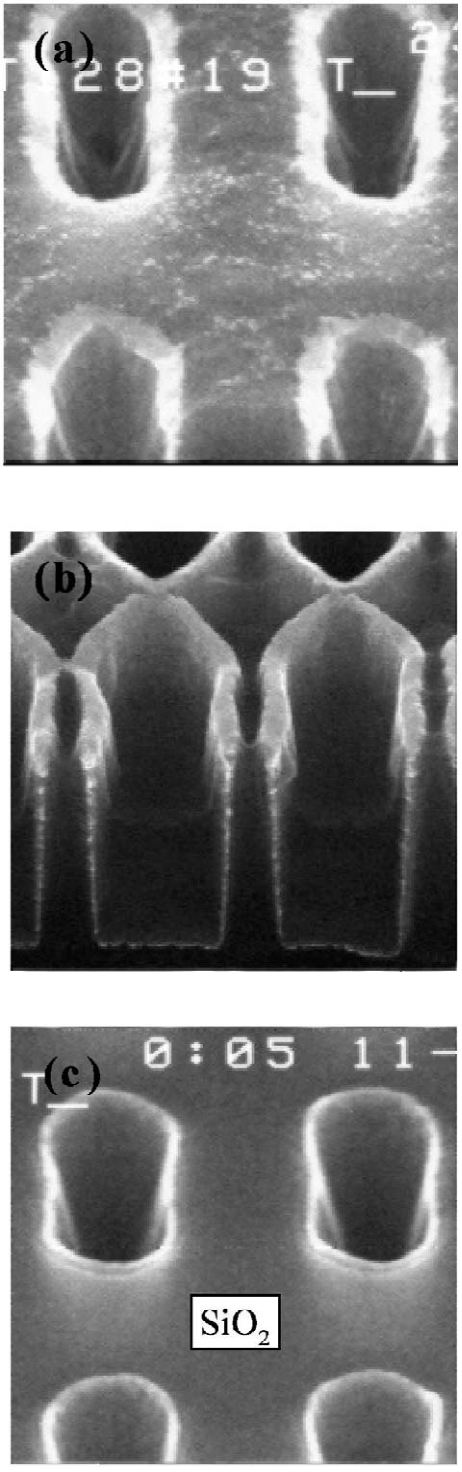

Fig. 7. Change of the profiles depending on the over-etch conditions. (a) After the etch process only. (b) After the over-etch process with a SiO_2 to Pt etch selectivity of < 1. (c) After the over-etch process with a SiO_2 to Pt etch selectivity of about 1.

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