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Patterning of W/WN_x/poly-Si gate electrode using Cl_2/O_2 plasmas

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Abstract

The metal gate electrode with a tungsten (W)/tungsten nitride (WN_x)/poly-Si structure has been successfully patterned by Cl_2/O_2 plasmas in a helicon etcher. The patterned metal gate electrode showed an almost vertical profile and no pitting of the gate oxide. The etch selectivity of W over polysilicon (poly-Si) increased with increasing source power, decreasing bias power, and increasing $O_2/(Cl_2 + O_2)$ gas flow ratio. We reveal that W etch rate enhances with increasing temperature.

Keywords: Tungsten; Metal gate; Etching; Temperature

1. Introduction

As device dimension becomes smaller, the gate resistance becomes higher and thus the usage of the metal gate electrodes with low resistivity should be considered. Also, depletion of gate electrode must be suppressed to increase the effective gate capacitance and improve the device characteristics of sub-0.10-μm metal-oxide-semiconductor field effect transistors (MOSFETs) [1].

The refractory metal gate electrodes such as W, titanium nitride (TiN), and tantallium (Ta) have been reported to be promising candidates to realize no gate depletion and low gate resistance [2–7]. Among the metallic gate materials, W has been considered appropriate due to its high thermal stability, good corrosion resistance, and high process compatibility.

In this paper, we report the patterning of metal gate electrodes with a W/WN_x/poly-Si structure. The poly-Si is inserted between W/WN_x and gate oxide because W/WN_x has a poor adhesion with the

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underlying gate oxide. The WN_x is inserted between W and poly-Si to prevent the generation of unwanted WSi_x layer.

We have employed a fluorine etchant (SF_6/HBr system) in preliminary experiments in order to pattern W/WN_x/poly-Si structures, revealing that the sidewall of poly-Si is locally eroded and pitting of gate oxide is observed due to low W to poly-Si etch selectivity of less than 0.3 (not shown here). Therefore, we suggest to increase W etch rate by forming WO_xCl_y etch product assisted by high ion bombardment using Cl_2/O_2 system in helicon wave plasma. We also investigate the etch selectivity of poly-Si over SiO_2.

2. Experimental

Schematic diagram of an $m = 0$ helicon plasma reactor used in this study is described in Fig. 1. Helicon wave plasma sources were operated at the excitation frequencies of 13.56 MHz. The diameter of the process chamber covered by 24 cusp magnets along the chamber axis was 350 mm. The helium pressure was 20 Torr and both the inner and the outer coil currents were 40 A. During etching, the source power was 500–2000 W, the bias power was 0–400 W, the magnetic field was 100–200 Gauss and the total gas flow rate of Cl_2/O_2 system was set to 50 standard cubic centimeters per minute (sccm).

The blanket wafers were used for measuring the etch rates of W, poly-Si and SiO_2, because the W/poly-Si and the poly-Si/oxide etch selectivity could not be measured accurately in patterned wafers. The patterned wafers with a critical dimension (CD) of 0.17 nm were used to demonstrate the formation of the metal gate electrode. Fig. 2 shows the cross-sectional view of metal gate electrode, with a structure of SiO_2 mask 2000 Å/W 1000Å/WN_x 100Å/poly-Si 1000 Å/gate oxide 60 Å/Si substrate.

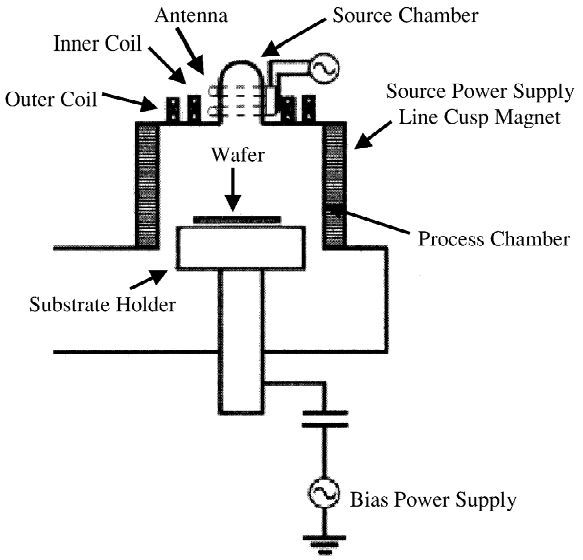

Fig. 1. Schematic diagram of an $m = 0$ helicon plasma reactor.

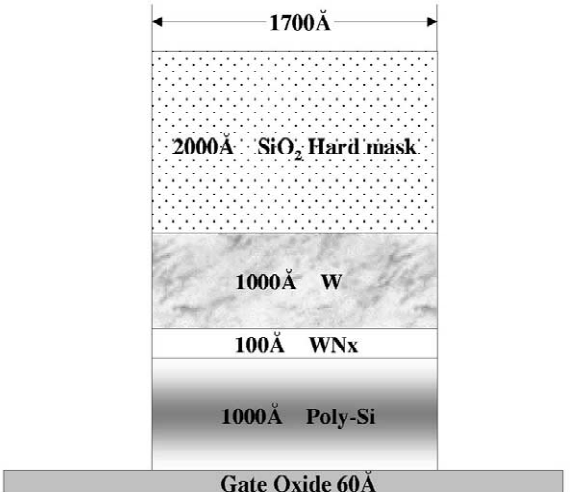

Fig. 2. Cross-sectional view of gate electrode pattern with a SiO_2 hard mask 2000 Å/W 1000 Å/WN_x 100 Å/poly-Si 1000 Å/gate oxide 60 Å.

The cathode temperature before etching was set to 20 °C by using a chiller. An irreversible thermal tape was used for measuring the wafer temperature in situ during etching processes. We attached the thermal tape on the surface of wafer and checked the indicated temperature by the thermal tape after etching process is completed. Because the wafer temperature depends on etching time, the etch time was fixed to 30 s in this study. A scanning electron microscope (SEM) (Hitachi S-4700) was used to evaluate the fabricated metal gate electrode.

3. Results and discussion

To investigate the feasibility of forming the W/WN_x/poly-Si structure with a vertical profile, etch rates of W and poly-Si were investigated by varying process conditions. Fig. 3 shows the variation of W etch rates, poly-Si etch rate, and etch selectivity of W over poly-Si with varying process parameters. The source power and the bias power ranges from 1000 to 2000 W and from 200 to 400 W, respectively. The pressure was 3–10 mTorr and the $O_2/(Cl_2 + O_2)$ gas flow ratio ranges from 0.2 to 0.6 with a total flow rate of 50 sccm. With increasing source power, the poly-Si etch rate decreases and the W etch rate increases, resulting in increase of the W to poly-Si etch selectivity. With increasing bias power, both poly-Si and W etch rates increase, resulting in slight decrease of W to poly-Si etch selectivity. W etch rate is maximized at O_2 and Cl_2 flow rates of 20 and 30 sccm, respectively, implying the possible formation of volatile WO_xCl_y compounds as an etch product. In spite of that, with increasing $O_2/(Cl_2 + O_2)$ gas flow ratio, the etch selectivity of W over poly-Si increases due to significant decrease of poly-Si etch rate. The W etch rate is considerably low at high (10 mTorr) pressure and increases with decreasing pressure.

Based on the above experimental results, we set up a standard etching condition in which the expected etch selectivity of W to poly-Si is about 1.4 and the expected etch selectivity of poly-Si to SiO_2 is about 9.7. At the standard etching condition the source power is 1500 W, the bias power is

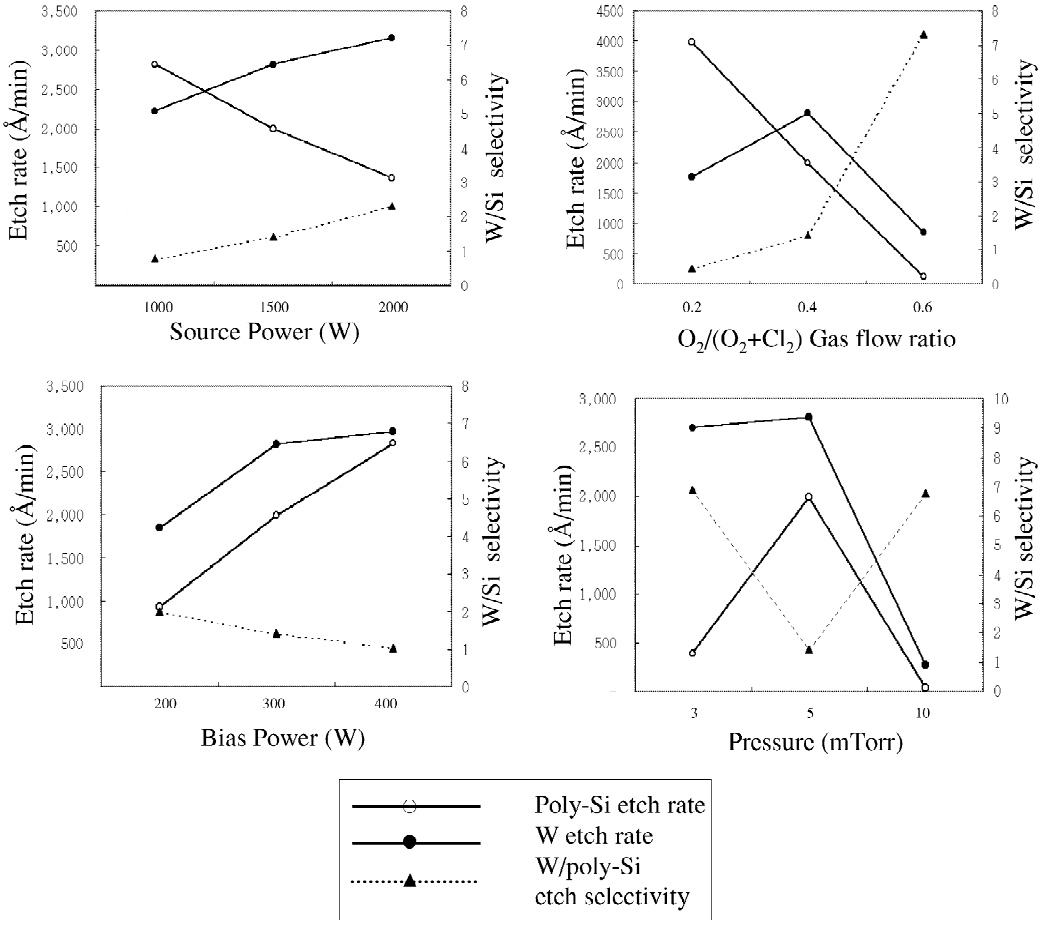

Fig. 3. Variation of W etch rates, poly-Si etch rate, and the etch selectivity of W over poly-Si with varying process parameters. The etch selectivity increases with increasing source power, decreasing bias power, and increasing O_2/Cl_2 ratio.

300 W, and the pressure is 5 mTorr, with a gas flow of $Cl_2/O_2 = 30{:}20$ (sccm) for 60 s. Fig. 4 shows the etch profiles of the gate electrode pattern measured from top, center and bottom regions of 8-inch wafers. Top three pictures indicate the cell pattern with a CD of 0.17 nm and bottom three pictures indicate the patterns in peripherial region. A straight and almost vertical etch profile without sidewall residues and defects is uniformly produced. We observe no post-etch pitting or defect of the gate oxide throughout the wafer.

With an expectation to apply into future devices with the ultra-thin gate oxide, we investigated the etch selectivity of poly-Si over SiO_2 with varying process parameters (see Fig. 5). With increasing bias power, the SiO_2 etch rate is almost invariant but the poly-Si etch rate increases, resulting in increasing etch selectivity of poly-Si over SiO_2. When the bias power is 200, 300, and 400 W, respectively, the etch selectivity is 7.8, 9.7, and 10.2. With increasing source power, the SiO_2 etch rate is almost invariant but the poly-Si etch rate decreases, resulting in decreasing etch selectivity of

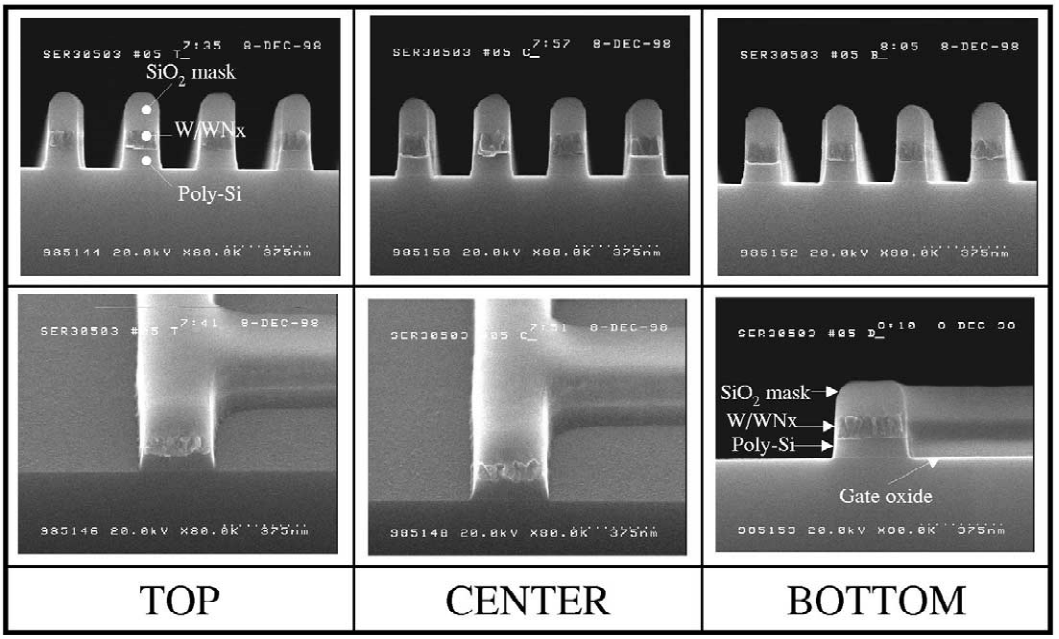

Fig. 4. Etching profiles of the gate electrode pattern in top, center and bottom region of 8-inch wafer. The source power is 1500 W, the bias power is 300 W, and pressure is 5 mTorr. The flow rates of Cl_2 and O_2 gases are 30 sccm and 20 sccm, respectively, for 60 s. The metal gate electrode shows a straight sidewall and no gate oxide pitting homogeneously. Top three pictures indicate the cell pattern with a CD of 0.17 nm and bottom three pictures indicate the patterns in peripheral region.

poly-Si over SiO_2. When the source power is 1000, 1500, and 2000 W, respectively, the etch selectivity is 14.8, 9.7, and 6.3. With increasing gas flow ratio of $Cl_2/(Cl_2 + O_2)$, the SiO_2 etch rate slightly increases but the poly-Si etch rate increases significantly, resulting in increase of poly-Si to SiO_2 etch selectivity. When $Cl_2/(Cl_2 + O_2)$ gas flow ratio is 0.4, 0.6, and 0.8, respectively, the etch selectivity is 0.7, 9.7, and 11.5. To sum up, the poly-Si to oxide etch selectivity improves with increasing bias power, with decreasing source power, and with increasing gas flow ratio of $Cl_2/(Cl_2 + O_2)$.

We measure the wafer temperature with varying process conditions using W blanket wafers (see Fig. 6). As the pressure decreases from 20 to 3 mTorr, wafer temperature increases from 85 to 180 °C. As the source power increases from 1000 to 2000 W, wafer temperature increases from 125 to 170 °C. As the bias power increases from 0 to 400 W, wafer temperature increases from 95 to 180 °C. From above observation, we reveal that wafer temperature increases with increasing source power, increasing bias power, and decreasing pressure. By comparing Fig. 6 with Fig. 3 regarding experimental results with varying source power, bias power, and pressure, we reveal that W etch rate increases with increasing wafer temperature.

We suppose that W etching process consists of chemical etching by radicals and physical sputtering by energetic ions. From the results of the O_2/Cl_2 gas ratio test in Fig. 3 shows that the optimum $Cl_2/(Cl_2 + O_2)$ gas flow ratio for maximal W etch rate exists, probably due to formation of volatile

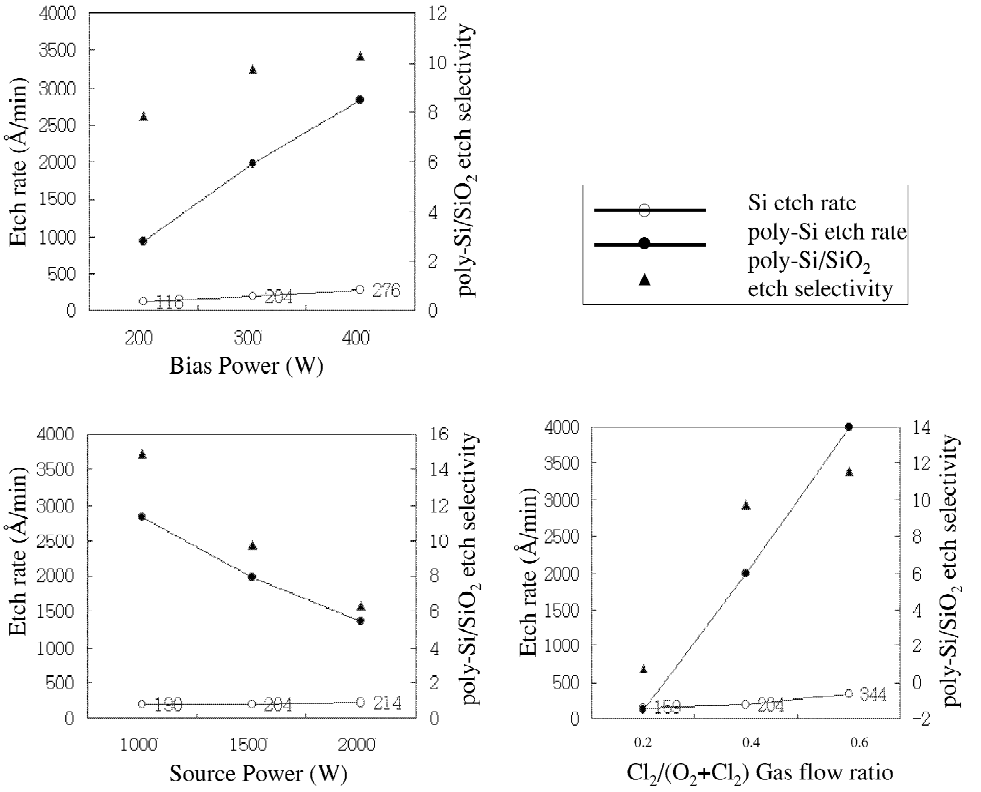

Fig. 5. Variation of the etch selectivity of poly-Si over SiO_2 with varying process parameters. The etch selectivity increase with increasing bias power, decreasing source power, and decreasing O_2 ratio in the Cl_2/O_2 system.

WO_xCl_y compounds from the reaction of W with the Cl and O species in plasma. We also surmise that the formation of WO_xCl_y compounds is crucial because the boiling point of $WOCl_4$ is about 227 °C and much lower than the boiling points or sublimation temperature of WCl_x and WO_x compounds. The enhancement of W etch rates with increasing temperature is possibly due to the enhancement of the compound-forming reaction at higher temperature. Also the physical sputtering by energetic ion may be crucial for efficient W etching not only because the sputtering assists the chemical reaction but because the ion bombardment and resulting temperature elevation help to desorb the volatile etch products. The detailed mechanism by which elevation of wafer temperature contribute to enhanced W etching needs to be investigated.

In order to reveal the effect of process parameters on W etching, source power and bias power are varied with other parameters fixed at standard etching condition. When the bias power is fixed to 100 W and the source powers are 500, 1000, and 1500 W, respectively, the W etch rate is 8, 14, and 36 Å/min. When the source power is fixed to 500 W and the bias powers are 100, 200, and 300 W, respectively, the W etch rate is 8, 90, and 1032 Å/min. Therefore, if bias power is low, W cannot be etched even at very high (1500 W) source power and if bias power is high, W can be etched even at very low (500 W) source power, revealing that bias power is one of crucial parameters in W etching. Further study is needed to disclose the effect of other parameters.

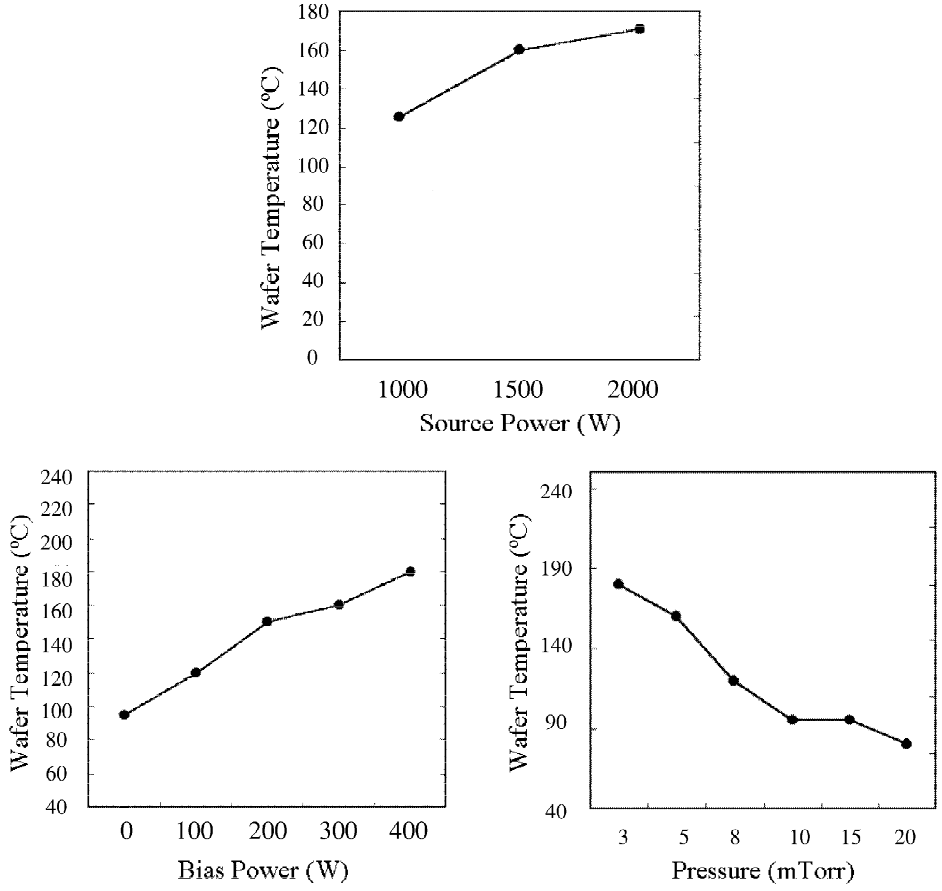

Fig. 6. Variation of the wafer temperature with varying process parameters.

4. Conclusion

We demonstrate the successful pattering of a W/WN_x/poly-Si structure using Cl_2/O_2 system in a helicon wave plasma. The fabricated metal gate electrode shows an almost vertical profile and no pitting of gate oxide homogeneously throughout the wafer. The etch selectivity of W over poly-Si increases with increasing source power, decreasing bias power, and increasing $O_2/(Cl_2 + O_2)$ gas flow ratio. The etch selectivity of poly-Si over SiO_2 increase with increasing bias power, decreasing source power, and decreasing $O_2/(Cl_2 + O_2)$ gas flow. We reveal that high wafer temperature is important for efficient W etching.

Acknowledgements

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